Transport or Store? Synthesizing Flow-based Microfluidic Biochips using Distributed Channel Storage

Chunfeng Liu¹,², Bing Li¹, Hailong Yao³, Paul Pop⁴, Tsung-Yi Ho²,⁵, Ulf Schlichtmann¹

1 Institute for Electronic Design Automation, Technical University of Munich, Germany
2 Institute for Advanced Study, Technical University of Munich, Germany
3 Tsinghua University, Beijing, China,
4 Technical University of Denmark, Denmark
5 Department of Computer Science, National Tsing Hua University, Taiwan
Overview

Motivation

Problem formulation and basic idea

Architectural synthesis with distributed channel storage

Results

Summary
From traditional labs to microfluidics

Traditional lab
- Large fluid sample volumes
- Slow reaction
- Bulky and expensive
- Error-prone

Flow-based biochip
[Elvira et al., 2013]

Digital biochip
[Abdelgawad and Wheeler, 2009]

- Lab-on-a-chip
- Small volumes
- Fast reaction
- High precision
Flow-based biochip operations

- Switches control flow paths.
- Channels can either transport or store.

Mixing and storing [Amin09]
Flow-based biochips: the electronic view

Our idea: Generating a new architecture for a given bioassay considering:

- Minimizing storage needs
- Introducing built-in distributed storage
Synthesized example

- No dedicated storage unit; channels used for either transportation or distributed storage
Problem formulation

- Input: sequencing graph of a biochemical assay
- Output: a schedule with storage reduction; a biochip with distributed storage and compact physical design
- Objective: minimizing overall resource usage; minimizing the execution time of the assay
Scheduling and storage requirements

- Storage lifespan $u_{ij} = \text{starting\_time\_of\_child\_operation} - \text{ending\_time\_of\_parent\_operation}$
- $u_c$: channel transportation time from $d_i$ to $d_j$
- $u_{ij} > u_c \& d_i \neq d_j \rightarrow$ storage requirement
Storage reduction in scheduling

Current solution:
ILP formulation, minimize: execution time $T$ and $\sum_{o_i \rightarrow o_j, d_i \neq d_j} u_{ij}$

Further HLS techniques will be applied.
Storage reduction example

Two storage requirements

One storage requirement
Channel network

- For fluid transportation, channels need to be built between devices.
- Channels may cross → nonplanar network → switches
Channel network with distributed storage

- Fluid caching in channel segments
- Distributed storage may be more efficient than a dedicated storage unit.
Build channel network from a virtual connection grid

- Synthesize chip architecture on a virtual grid
- Nodes: location options for devices or switches
- Edges: possible fluid transportation paths or storages
- Objective: minimize the number of used edges
- Current solution: ILP formulation
- Remove all nodes and edges not used → chip architecture
Iterative physical design

• Iterative physical design due to the planarity of the chip architecture
• Lengths of channel segments should be maintained so that fluid samples can be stored.
Synthesized example
Execution time and valve usage improvement

- Execution time and the number of valves ratio from our method to the architecture with dedicated storage (lower is better; lower than 1 means improvement.)
Summary

- A biochip architecture with distributed storage
- Storage reduction in assay scheduling
- Transportation channels and storage channels are modelled on a virtual grid.
- More efficient execution of the biochemical assay with even fewer resources
Thank you for your attention!