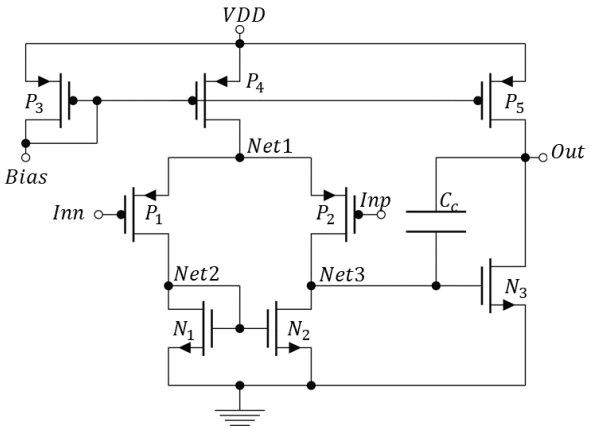
Master Thesis/Bachelor Thesis/Internship

Implementation of the EKV transistor model in an automatic initial sizing tool for analog circuits



Analog circuits are a major part in integrated systems. However, the design automation lacks behind the digital one. To automate the initial sizing of analog circuits, a tool is developed at the Institute of Design Automation.

In the moment this tool is based on the Shichman-Hodges transistor model, a very simple model. However, the simplicity of the model leads to mismatches with simulation results. To overcome this problem, a more accurate transistor model shall be used in the automatic sizing tool – the EKV model. The EKV model needs less parameter as for example the BSIM model to obtain similar accuracy, so it is much easier to be implemented in the automatic sizing tool.

Task:

- Analyzing the parameters and equations of the EKV model
- Implementation of the EKV model in the existing tool
- Verification of the model by comparison with simulation results in Cadence

Requirements:

- Interest or experience in analog circuits
- Basic knowledge of C++ advised
- Familiar with Cadence Virtuoso

If you are interested please contact me:
Inga Abel (inga.abel@tum.de).